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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,843	05/25/2000	Tetsushi Sato	Q59385	6287

7590 03/31/2004  
Sughrue Mion Zinn MacPeak & Seas  
2100 Pennsylvania Avenue NW  
Washington, DC 20037-3202

EXAMINER

CHANG, KENT WU

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/577,843

Applicant(s)

SATO ET AL.

Examiner

Kent Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3, 5, 6.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 6, 7, 12, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada (JP07-134277) in view of Kanba (JP10-334685).

Asada discloses a scanning circuit for a panel display comprising a bi-directional shift register and a feedback circuit controlled by four phase clocks, wherein the feedback circuit having a first inverter and a clocked second inverter (see pages 4-5). Asada is silent in using a delay circuit in delaying the control clock provided to the transfer gate.

However, Kanba teaches to use a delay circuit in delaying the control clock supplied to a feedback circuit (the latch) in a shift register (Paragraph 2-3 on page 2). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to use a delay circuit in delaying the control clock supplied to a feedback circuit in a shift register as taught by Kanba in the device of Asada so as to prevent malfunctions and stabilize the operation of the system.

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3. Claims 3, 5, 8, 9, 10, 11, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada (JP07-134277) in view of Kanba (JP10-334685) and Kihara et al (JP10-74062).

Asada discloses a scanning circuit for a panel display comprising a bi-directional shift register and a feedback circuit controlled by four phase clocks, wherein the feedback circuit having a first inverter and a clocked second inverter (see pages 4-5). Asada is silent in using a delay circuit in delaying the control clock provided to the transfer gate.

However, Kanba teaches to use a delay circuit in delaying the control clock supplied to a feedback circuit (the latch) in a shift register and supplying both the transfer part and the feedback circuit part with clocks supplied from the same input clock (Paragraph 2-3 on page 2). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to use a delay circuit in delaying the control clock supplied to a feedback circuit in a shift register as taught by Kanba in the device of Asada so as to prevent malfunctions and stabilize the operation of the system.

Kihara teaches a phase control circuit for determining the data shifting direction in a bi-directional shift register (see page 1). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to use a phase control circuit for determining the data shifting direction in a bi-directional shift register as taught by Kihara in the device

of Asada as modified so as to provide direction shifting to the circuit with simple design and operation.

4. Claims 3, 5, 8, 9, 10, 11, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada (JP07-134277) in view of Kanba (JP10-334685) and Asada (JP05-35213).

Asada (JP07-134277) discloses a scanning circuit for a panel display comprising a bi-directional shift register and a feedback circuit controlled by four phase clocks, wherein the feedback circuit having a first inverter and a clocked second inverter (see pages 4-5). Asada is silent in using a delay circuit in delaying the control clock provided to the transfer gate. However, Kanba teaches to use a delay circuit in delaying the control clock supplied to a feedback circuit (the latch) in a shift register and supplying both the transfer part and the feedback circuit part with clocks supplied from the same input clock (Paragraph 2-3 on page 2). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to use a delay circuit in delaying the control clock supplied to a feedback circuit in a shift register as taught by Kanba in the device of Asada so as to prevent malfunctions and stabilize the operation of the system.

Asada (JP05-35213) further teaches a shift register wherein the feedback circuit is provided with a second inverter connected through a transfer gate along with a first inverter (Fig.1 on page 1). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention

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to use a shift register wherein the feedback circuit is provided with a second inverter connected through a transfer gate along with a first inverter as taught by Asada (JP05-35213) in the device of Asada as modified so as to provide a high-yield, high speed scanning circuit as suggested by Asada.

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Margolin (US Patent No. 4,195,293); Nishimichi (US Patent No. 5,287,025); Saito et al (US Patent No. 6,232,939).

### **CONTACT INFORMATION**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent Chang whose telephone number is 703-305-4824. The examiner can normally be reached on Monday to Thursday from 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached at 703-305-4938.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

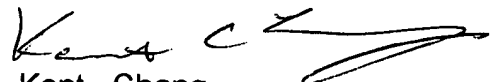
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**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121

Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 305-9700.



Kent Chang  
Primary Examiner  
Art Unit 2673

Kc

3/21/04